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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
9319I-000647

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

On August 6, 2007

Signature _____

Typed or printed name G. Gregory Schivley / Bryant E. Wade

Application Number	Filed
10/757,373	January 14, 2004
First Named Inventor: HARA, Kazumi	
Art Unit: 2826	Examiner: Alexander O. Williams

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

X

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☒ attorney or agent of record.
Registration number 27,382 / 40,344.

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Signature

G. Gregory Schivley / Bryant E. Wade
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(248) 641-1600
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August 6, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/757,373
Filing Date:	January 14, 2004
Applicant:	HARA, Kazumi
Group Art Unit:	2826
Examiner:	Alexander O. Williams
Title:	SEMICONDUCTOR CHIP AND SEMICONDUCTOR WAFER INCLUDING A VARIABLE THICKNESS INSULATING LAYER
Attorney Docket:	9319I-000647

Mail Stop AF
Commissioner for Patents
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Alexandria, Virginia 22313-1450

APPLICANT ARGUMENTS CORRESPONDING TO PRE-APPEAL BRIEF REQUEST FOR REVIEW

In conjunction with Applicant's Pre-Appeal Brief Request for Review, Applicant contends that there is no suggestion to modify the teachings of Siniaguine (U.S. Pub. No. 2002/0084513), and that there is no suggestion or motivation to modify the teachings of Siniaguine with the teachings of Patti (U.S. Pub. No. 2004/0048459) because the cited references fail to teach or suggest all the elements of the presently pending claims.

STATUS OF CLAIMS

Claims 5-8, 34, and 42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Siniaguine (U.S. Pub. No., 2002/0084513). Claims 19-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Siniaguine in view of Patti (U.S. Pub. No. 2004/0048459).

SUMMARY OF CLAIMED SUBJECT MATTER

Independent Claim 1 recites a semiconductor chip comprising a semiconductor substrate, and an integrated circuit. At least a part of the integrated circuit is formed in the semiconductor substrate. A penetrating electrode is formed in a through-hole of the semiconductor substrate from a first surface to a second surface of the semiconductor substrate. The through-hole has sidewalls entirely orthogonal to the first and second surface, and the penetrating electrode has a projection which projects from the second surface. An insulating layer is formed over an entire surface of the second surface of the substrate. The insulating layer includes a first insulating section formed in a region that surrounds the projection such that the projection forms a through-bore in the first insulating section above the second surface of the substrate, and a second insulating section that covers a remaining region of the second surface of the semiconductor substrate. The first insulating section is connected to the second insulating section by a radially tapering arcuate portion having a varying radius of curvature from the through-bore to the second insulating section. The second insulating section is formed to be thinner that a thickest area of the first insulating section.

Independent Claim 19 recites a semiconductor wafer comprising a semiconductor substrate, and a plurality of integrated circuits. At least a part of each of the integrated circuits are formed in the semiconductor substrate. A plurality of

penetrating electrodes are formed in through-holes of the semiconductor substrate from a first surface to a second surface of the semiconductor substrate. The through-holes have sidewalls entirely orthogonal to the first and second surface, and the penetrating electrodes each have a projection which projects from the second surface. An insulating layer is formed over an entire surface of the second surface of the substrate. The insulating layer includes a plurality of first insulating sections and a second insulating section other than the first insulating sections. Each of the first insulating sections are formed in regions that surround the projections above the second surface of the substrate such that the projection's defined through-bores in the first insulating section, and the second insulating section covers a remaining region of the second surface of the semiconductor substrate. The first insulating sections are connected to the second insulating section by radially tapering arcuate portions having a varying radius of curvature from the through-bore to the second insulating section. The second insulating section is formed to be thinner than a thickest area of each of the first insulating sections.

ARGUMENT

Claim 5 recites a semiconductor chip having a "first insulating section being connected to the second insulating section while radially tapering arcuate portion having a varying radius of curvature from the through-bore to the second insulating section." The Examiner alleges that a semiconductor device as recited in Claim 5 is obvious in view of Figures 8 and 10-12 of Siniaguine. Referring to Figure 8 of Siniaguine, a dielectric layer 140 having an alleged tapering portion at 140P is illustrated. The tapering portion 140P, however, does not include a radially tapering arcuate portion having a varying radius of curvature from the through-bore to the second insulating section, as claimed. In contrast, the teachings of Figure 8 merely

show an angled connection. An angled connection, however, does not yield the claimed "radially tapering arcuate portion having a varying radius of curvature from the through-bore to the second insulating section."

Additionally, although Siniaquine allegedly teaches a polyimide layer 710 in Figure 12 that completely covers a second surface of the substrate 110, Figure 12 also fails to teach the claimed radially tapering arcuate portion. Again, the teachings of Figure 8 merely show an angled connection. An angled connection, however, does not yield the claimed radially tapering arcuate portion having a varying radius of curvature from the through-bore to the second insulating section. Because this feature is neither taught nor suggested by Siniaguine, Applicant respectfully asserts that the Examiner has not established a prima facie case of obviousness with respect to Claim 5. That is, each and every limitation of the claimed invention is neither taught nor suggested by Siniaguine.

The Examiner has also failed to establish a prima facie of obviousness for Claim 19. Claim 19 recites a semiconductor wafer having a "first insulating section being connected to the second insulating section by radially tapering arcuate portions having a varying radius of curvature from the through-bore to the second insulating section." As stated above, Siniaguine fails to teach a radially tapering arcuate portion having a varying radius of curvature from the through-bore to the second insulating section. Patti is also silent with respect to this aspect of the claimed invention. Because neither Siniaguine nor Patti teach or suggest this feature of the claimed invention, Applicant respectfully asserts that the Examiner has failed to establish a prima facie case of obviousness with respect to independent Claim 19.

Furthermore, Applicant respectfully asserts that the Examiner has failed to address these arguments presented in the Response to Office Action filed June 26, 2007 in the Advisory Action mailed July 27, 2007. As argued in the Response, the cited art fails to teach a radially tapering arcuate portion because the insulating layer 140 merely includes an angled tapered portion. By failing to rebut this argument, Applicant respectfully asserts that the Examiner has acquiesced in Applicant's position that such a feature is absent from the cited art. Accordingly, Applicant further asserts that the Examiner's silence on this matter further supports the position that a prima facie case of obviousness has not be established.

Respectfully submitted,

Dated: August 6, 2007

By: _____

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